Abstract of the Disclosure

A semiconductor memory device features a nonvolatile ferroelectric mode register. In the semiconductor memory device, a reset process of the mode register is not required in a power-up mode. Additionally, the semiconductor memory device comprising a nonvolatile ferroelectric mode register can perform the same operation as that of SDR (Single Data Rate) SDRAM (Synchronous Dynamic Random Access Memory) or DDR (Double Data Rate) SDRAM. Accordingly, in the semiconductor memory device, data stored in the mode register can be maintained in a power-off state, and the compatibility with DRAM can be obtained.